WHAT IS CLAIMED IS:

1. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected gate formed of a silicon carbide material.

2. The transistor of claim **1**, wherein the gate comprises polycrystalline silicon carbide.

3. The transistor of claim **1**, wherein the gate comprises microcrystalline silicon carbide.

4. The transistor of claim **1**, wherein the transistor is a p-channel device.

5. The transistor of claim **1**, wherein the transistor is an n-channel device.

6. The transistor of claim **1**, wherein the silicon carbide gate material is described by $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5

7. The transistor of claim **6**, wherein X is approximately equal to 0.5.

8. The transistor of claim **1**, wherein the gate is separated from the channel by an insulating layer.

9. The transistor of claim **8**, wherein the insulating layer is approximately between 50 angstroms and 100 angstroms thick.

10. The transistor of claim **8**, wherein the insulating layer is approximately 100 angstroms thick.

11. An integrated circuit device comprising:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer.

12. The integrated circuit device of claim **11**, wherein the p-channel and n-channel silicon carbide gates comprise polycrystalline silicon carbide.

13. The integrated circuit device of claim **11**, wherein the p-channel and n-channel silicon carbide gates comprise microcrystalline silicon carbide.

14. The integrated circuit device of claim **11**, wherein the insulating layers, which separate the silicon carbide gates in each of the n-channel and p-channel transistors from their respective channel regions, are comprised of silicon oxide.

15. A semiconductor memory device comprising:

a memory array including a plurality of transistors, at least one of the transistors including an electrically interconnected gate formed of a silicon carbide material;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

16. A method of fabricating a transistor, the method comprising the steps of:

fabricating source and drain regions in a substrate, a separation between the source and drain regions defining a channel region;

fabricating an insulating layer overlying the channel region; and

fabricating an electrically interconnected silicon carbide gate on the insulating layer.

17. The method of claim **16**, wherein fabricating the silicon carbide gate includes the steps of :

depositing a layer of silicon carbide material on the insulating region using low pressure chemical vapor deposition; and

etching the silicon carbide material to a desired pattern using a reactive ion etch process.

18. The method of claim **17**, wherein etching the silicon carbide material further includes using plasma etching in combination with the reactive ion etching.

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~~20~~. The method of claim **18**, further comprising the step of oxidizing the silicon carbide material to form a thin layer of oxide on the silicon carbide material.

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~~21~~. The method of claim **17**, wherein the insulating region has a thickness of approximately 100 angstroms.

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~~22~~. The method of claim **17**, wherein the insulating region has a thickness of approximately between 50 angstroms and 100 angstroms.

Rule 1.126

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